## REMARKS AND ARGUMENTS

### Status of the Application

Claims 1-24 are pending in the subject application. Claims 23-24 are objected to by the Examiner and claims 1, 13-14 are rejected under 35 USC § 102. Claims 2-12, 15-24 are objected as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. By way of this amendment, Applicant has cancelled claims 1, 4, 5, 8 and 24 without prejudice and added new claims 25-33.

### Objections to Claims

Claims 23 and 24 are objected to by the Examiner. In particular, the term "the testing" in claims 23 and 24 should be amended to "testing circuit" as defined by claim 21. In response, Applicant has amended claim 23 to delete the term "testing" while claim 24 has been cancelled. Therefore, the Applicant submits that the objections to the claims are either moot or have been traversed and requests their withdrawal.

Claims 2-12 and 15-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, Applicant has amended claim 2 to be in independent form to include all of the limitations of the base claims and any intervening claims. As for claim 15, Applicant has amended it to include all limitations of the base claim and any intervening claims except for the limitation recited in intervening claim 13. Applicant submits that the limitation recited in claim 13, which is that a memory bank comprises at least one

memory sub-array, is not material for patentability of claim 15. Applicant submits that claims 2 and 15 are now patentable over the cited art of record. Claims 4, 5, 8 and 24 have been cancelled by this amendment and the objections to these claims are therefore moot. Since claims 3, 6-7, 9-12, 16-23 are either directly or indirectly dependent on claim 2 or 15, these claims are also patentable.

**Rejection under 35 USC §102**

Claims 1, 13-14 are rejected under 35 USC § 102(e) as being anticipated by Nakamura (US Patent No. 6,523,135). Applicant respectfully disagrees. However, claim 1 has been cancelled and claims 13-14 are directly or indirectly dependent on claim 2, which has been amended to overcome the objection, as discussed already. Therefore, Applicant submits that rejections based on 35 USC §102 are either moot or traversed, and respectfully requests their withdrawal.

As for newly added claim 25, it recites an integrated circuit having a memory array which includes a plurality of memory banks and a BIST for testing the memory array. A plurality of comparator units are provided, wherein at least one comparator is associated with one memory bank. The plurality of comparators facilitates parallel testing of the memory banks simultaneously.

Nakamura teaches the use of a BIST circuit that is built in a DRAM for testing the function of a DRAM. However, Nakamura nowhere mentions or suggests the use of a memory array separated into a plurality of banks nor testing the plurality of banks of the DRAM in parallel with the BIST circuit. In fact, Applicant submits that the BIST circuit of Nakamura is incapable of testing a plurality of memory banks in parallel. In particular, the BIST circuit of

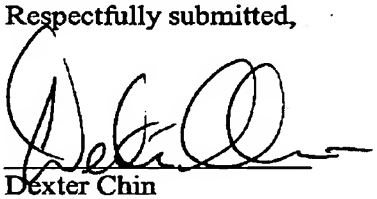
Nakamura includes write, read and read/write circuits for performing write, read and read/write tests, respectively. *See* Nakamura at col. 3, lines 13-20 and col. 4, lines 28-52. The read and read/write circuit each includes a single comparator. *See* Nakamura, Figs. 2 and 3. When a read test is performed, the comparator in the read circuit compares the read data with the expected data. *See* Nakamura at col. 5, lines 37-40. On the other hand, the comparator of the read/write circuit compares the read data and the expected data when a read/write test is conducted. Since only one comparator is used during a specific test mode (e.g., read or read/write), only one address can be tested at a time. Therefore, the BIST circuit of Nakamura cannot test multiple banks in parallel, as presently recited in claim 25. As such, claim 25 is patentable over Nakamura. Since new claims 26-33 are directly or indirectly dependent on claim 25, these claims are also patentable.

**Conclusion**

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance and the issuance of a formal Notice of Allowance at an early date is respectfully requested. Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Date: February 16, 2004

Respectfully submitted,



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